300 mm Conversion Timing

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Abstract: Periodic increases in wafer size have been a principle component of the semiconductor industry's unmatched growth in productivity. The conversion from 200 mm to 300 mm wafers, while undergoing some timing adjustment to business conditions in the late 1990s, will occur on a schedule consistent with historic trends. Analysis of previous wafer size life cycles yields a model profile for a typical wafer generation relative to prior and subsequent sizes. The extrapolation of this historic model agrees with forecasts of wafer demand and size transition based on future semiconductor market growth projections. The demand side of the conversion must be balanced by the availability of a full set of capable 300 mm equipment and materials for the industry to remain on its historic productivity curve. Device companies, their suppliers and global consortia, recognizing this dependency, are supporting the transition with unprecedented cooperation.

Introduction

The semiconductor industry has grown rapidly to become a major driver of the world economy. Its customers have received a doubling of product performance every 18 months for the same cost, a trend embodied in Moore's Law. This 25% to 30% per year decrease in cost per function has driven demand in a classic display of market elasticity. To continue this productivity and business growth, the industry has improved several key elements in its manufacturing operations. The largest contribution to technical performance has historically come from steadily reducing lithographic feature sizes to increase the speed of devices. Increasingly effective control of defect density and processing variability has improved product yields to very high levels soon after factories start up. Efficient use of manufacturing assets has been improved by higher equipment throughput and reliability, as well as by integrated factory information and control systems. Periodic wafer size increases have provided lower cost per unit area of silicon by significantly increasing area output from factories that cost moderately more than ones for previous wafer sizes.

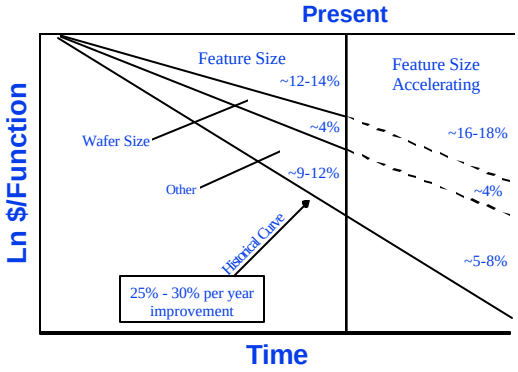

Figure 1. Productivity improvement components

There have been characteristic rates of change for the elements of productivity improvement. While macroeconomic business cycles and industry demand/capacity mismatches have caused some variation in timing, a new generation or node of device technology has generally developed every three years. Recent acceleration of lithographic capability has decreased the periods for change between 0.35, 0.25 and 0.18 micron nodes closer to two years [1]. Aggressive shrinking of chip size to reduce manufacturing cost and scaling of critical layers for performance have driven this acceleration. Despite this feature size reduction, increasing levels of functionality have resulted in steady growth in chip size, with the number of die on each wafer driving the economics of wafer size

The cadence and life cycles characteristic of larger wafer size introductions has also responded to business conditions, but can be described by models which account for the continuing growth of the industry and the need to minimize manufacturing cost and capital investment. The conversion to 300 mm wafers, while responding to current business conditions, is occurring in the timeframe projected from analysis of historic trends and future demand.

Demand-based Transition Analysis

Due to increasing awareness of the inter-

dependence of their activities, there has been an much interest within the semiconductor supplier and manufacturer communities to develop a common framework for the timing, rate, and magnitude of the mutually-shared wafer conversion process. Models have been developed at SEMATECH and I300I to attempt to forecast the most productive conversion of future market product demand from the 200 mm wafer generation to the 300mm wafer generation. To help validate the demand-based conversion model, past historical wafer generations were analyzed and models developed of the historical conversions.

The primary goal of the product-demand-driven model is to develop a credible scenario for the emergence of the 300mm production capability which would be consistent with historical trends and also represent the most productive utilization of manufacturing resources. From an industry productivity standpoint, the ideal model should satisfy the product demand "just-in-time" with the fewest semiconductor fabricator facilities (fabs} built per generation. For purposes of the fab demand forecast model, a "fab" is defined to have a 20,000 wafer-start-per-month (wspm) capacity. Mature yields were also assumed at 95% line yield, 80% probe yield, 99% assembly yield, and 90% final test yield, giving a 67% overall yield.

DRAM product demand was used to develop the model, since that product has historically represented 60% of the leading-edge production capacity. Unit volume history is readily available through subscription to services of major semiconductor analysts such as Dataquest, In-Stat, and Integrated Circuits Engineering (ICE). The unit volume historical data for the model results discussed in this article is shown graphically in figure 2 [2]. The historical graph clearly shows the cyclical nature of the DRAM generations, which typically start at three-year intervals, and peak within 6 years as successor generations become more competitive in pricing. The latest unit volume cycles shapes were projected forward to use as an example for the fab demand forecast for the 300mm conversion.

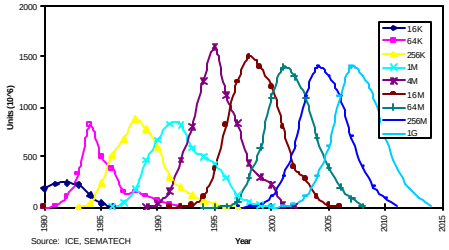

Figure 2. DRAM Unit Volume by Generation (Source: ICE, SEMATECH)

Also fundamental to the model are the die-per-wafer assumptions. For simplification, a simple wafer mapping model was used which assumed 88 square field exposures were available on each generation's circular area. The wafer field exposure map was laid out as 6 rows of 10 squares, 2 rows of 8 squares, and 2 rows of 6 squares. The field size of the exposure is a square which is approximately ten percent less than one-tenth of the diameter of the generation. For a 200 mm wafer this assumption results in 18 mm-square field, and a 27-mm square field for a 300mm wafer. A typical wafer exposure field layout is shown in figure 3.

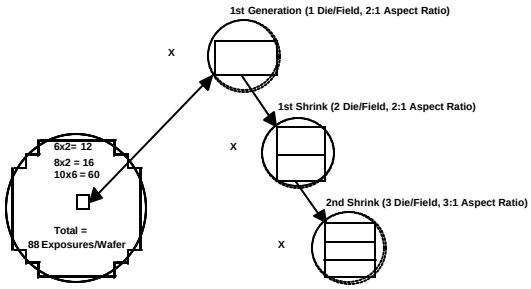

Figure 3. DRAM Die Area Model

Also seen in the figure is the die area model assumption that volume production ramp begins with two die per field at a 2:1 aspect ratio, which shrinks within two years to 3 die per field at a 3:1 aspect ratio. That second shrink supplies the target total die per wafer start of 264 (3x88), and a net monthly finished product output per fab of 3.6 million units (264 die per wafer x .67 overall yield x 20,000 wspm). This simple capacity model compared favorably with fab capacity of new construction announcements by major DRAM manufacturers.

Using the most recent data on 4M and 16M

DRAM die sizes, and the SIA National Technology Roadmap for Semiconductors (NTRS) forecast die sizes for 64M and up, the DRAM generations can be matched for timing with wafer generations. The 4Mb generation overlapped both 6" and 8", and drove the ramp-up of the 8" wafer generation. The 16Mb generation is clearly in the "sweet-spot" of the 8" wafer generation, while the start of 64Mb coincides with the conversion to 300 mm.

The large die area forecast for the 256M DRAM generation is a better fit for the die area/field size model of the 12"/300mm generation. Targeting the 12"/300mm model to begin pilot production in 1998 achieves lower cost for the entire 256M DRAM generation on the larger wafers. The 64M DRAM generation will most likely populate the mature 8" phase and also drive the leading-edge ramp of the 12" wafer generation, just as 4M drove the ramp of the 8" generation in the early 90's. Undoubtedly some portion of the 256Mb DRAM demand will be met by 8" fabs in spite of the unproductive use of the area by the large die, but the idealized model assumes that all 256M demand met by 12" capacity in order to build the fewest fabs that meet demand.

The timing and magnitude of the DRAM fab demand model shown in figure 4 indicates that about 50 fabs are required to meet the leading-edge product demand. Total fabs required at the leading edge can be estimated by assuming the DRAM demand represents about 60% of the capacity, implying that about 90 to 100 fabs are required to support other leading-edge product demand such as microprocessors, SRAM, chip-sets, high-performance embedded controllers, DSPS, and ASICS.

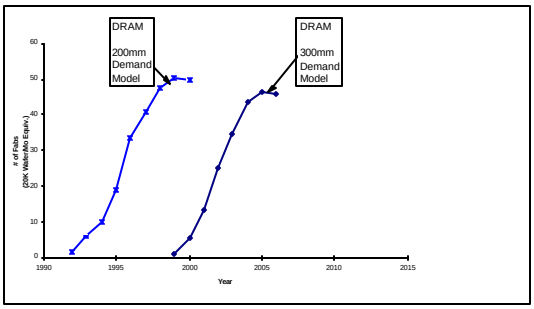

Figure 4. DRAM Fab Demand Model (Source: ICE, SEMATECH)

The fab demand model data output, combined with estimates of test wafer utilization ratios and fab ramp timings can be used to estimate the amount of silicon required at the leading edge ramp of the 200 mm and 300mm wafer generations and provide forecast timing and magnitudes for material and equipment demand. A two-year fab capacity ramp from pilot to full production, and typical test to product wafer ratios were used. The demand-based projection for 300 mm wafer area can then be compared to the historical wafer generation area trends, discussed next.

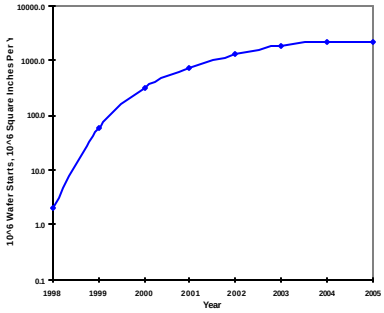

Figure 5. 300 mm Wafer Area Demand Model

Historical Conversion Trend Analysis

In order to validate the demand-based model of the 300mm wafer generation conversion, a broader context for past trends in the semiconductor industry is needed. To supply that context, it was necessary to analyze data over a greater historical range. Fortunately, a database of the wafer generation area and units has been preserved by Dan Hucheson at VLSI Research back to the early 1960's.

Analysis of historical data [3] reveals long-term trends in silicon consumption and characteristic life cycles for wafer size generations. Figure 6 shows the total semiconductor wafer area consumption history, indicating that after an initial rapid growth phase of the industry in the late sixties and into the seventies, the trend has maintained a compound annual growth rate of approximately 10%. This average rate has been consistent from the late seventies forward, despite periods where the market and economic environment caused cyclical oscillations around the trend.

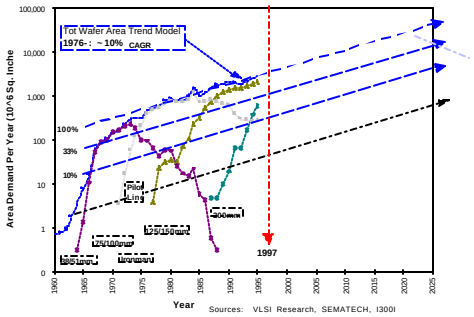

Figure 6. Cumulative Wafer Area History

Analysis of the individual cycles which make up the macro trend yields additional insights. For example, the wafer generations of the sixties and seventies ramped more quickly and had shorter life cycles than their successors. In addition, it can be observed that the generations tended to "cluster" in groups of two generations which were 3-years apart, with 6-year spacing between pairs. As wafer diameters continued to increase, and progress was made on fab yields and productivity, the industry shifted from closely-spaced pairs to single wafer size generations. The 5"/6" (125 mm/150 mm) doublet was the last to show this cluster characteristic. Increased industry productivity, coupled with an industry economic down cycle in the mid-eighties, resulted in a diminished peak and a shortened life for the 5" generation. Combining the 5" and 6" data results in a generation profile which can be used as a template for succeeding single-wafer generations, starting with the 8" (200 mm) generation.

By closer scrutiny of the wafer generation cycles, four distinct life-cycle phases can be identified. These are shown in Fig. 7, laid out upon the 5"/6" generation volume timing and compared to the overall area growth trend. The first phase is identified as the Leading-edge Phase spans about six years and is characterized by rapid growth rate to 33% of total area, at which time it forces the peaking of its preceding wafer generation, the 3"/4" (76/100 mm) pair. Next comes the Emerging Phase, which runs about 9 years and is characterized by a period of decelerating growth rate to the generation peak. During the Emerging Phase, the preceding 3"/4" generation is passed and peak area is reached. After the peak, the generation enters into the Mature phase, and a declining rate will be caused by the emergence of the new successor generation, (8"/200). During the Mature phase, capacity from earlier generations (3"/4") is absorbed, causing the End-of -Life of that generation pair.. The Mature phase lasts about 9 years, at which time the peak of the successor (8") occurs and another generation (12"/300mm) emerges, causing the onset of End-of Life.

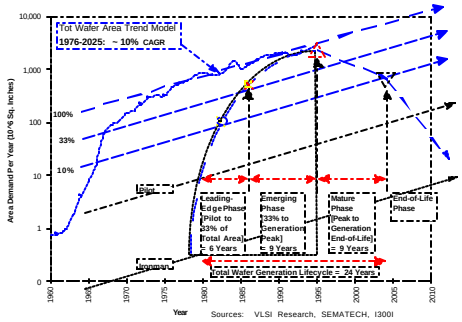

Figure 7. Wafer Generation Life Cycle Phases

The characteristic shape of the resulting model can be used as a cyclical template to compare to the recent 8"/200 mm generation trend data. When this is done (see figure 8), the 8" ramp begins on schedule for a 9-year cycle, but exhibits a volume lag in the early nineties. This delay can be attributed to the economic down cycle that occurred during that period. In the past three years, the 8" data appears to be accelerating back to the model levels.

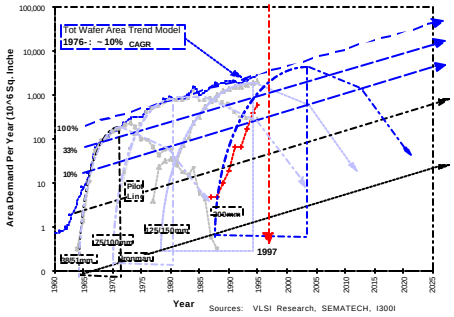

Figure 8. 200 mm Wafer Generation Life Cycle

Application of the model trend to the next nine-year cycle starting point suggests that the 12"/300mm should begin its pilot line start point about 1998. The demand model-based 300 mm generation wafer area curve aligns reasonably well with the model timing and ramp rate. It is evident that the demand-based model aligns best with the 6-year Leading-edge phase of the 12" generation.. If the 12" model forecast holds the generation should peak in 2013, and will not

reach End-of-Life until 2022.

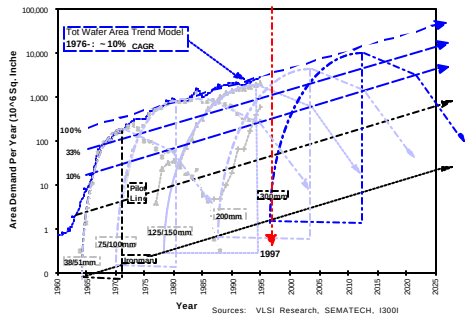

Figure 9. 300 mm Wafer Generation

Semiconductor manufacturer and supplier industries should benefit from both increased productivity and also a long period of return on the collective multi-billion dollar investment required to develop the 300 mm wafer substrate.

Plans of Device Companies

The semiconductor device manufacturers will build 300 mm factories to reduce manufacturing cost and to keep pace with the growth of their business. Projections of manufacturing cost of 300 mm fabs for 0.25 micron high performance logic and memory devices range from 30% to 40% lower than 200 mm fabs with equivalent wafer volumes [4,5]. A large, growing company can build a 300 mm factory every 18 to 24 months instead of building a 200 mm factory every year, with commensurately lower project and human resources. Several industry groups, including trade organizations, market research firms and consortia of device companies, have surveyed the specific plans for start-up of 300 mm facilities [6,7].

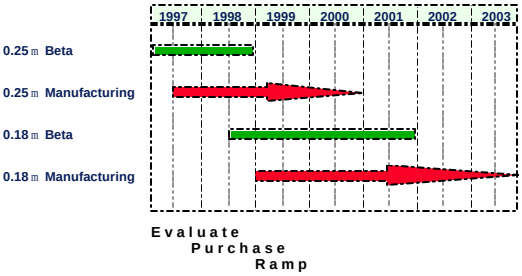

Figure 10. I300I Member Company Equipment Timing

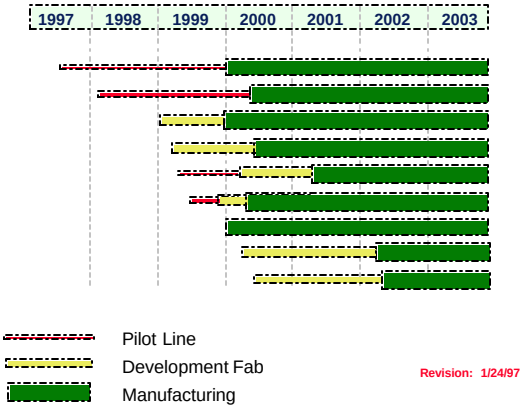

Figure 11. I300I Member Company Facility Start-up

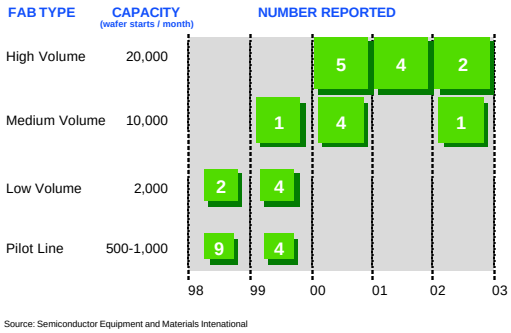

Figure 12. SEMI Global Device Company Timing Survey

The portrait that emerges from these surveys matches the projections of the models: pilot lines and development fabs will begin in 1998, with manufacturing operations beginning to ramp in 1999. Early in the next decade, most new fabs will be 300 mm.

Plans of Equipment and Materials Suppliers

To develop cost-effective equipment and materials for 300 mm, suppliers must have information on how factories will operate. They must also understand the expected levels of performance for key technical and manufacturing parameters. The device companies have worked together to achieve consensus in these areas, and have provided guidelines and metrics to address these needs. To meet the customer's plans for early operations in 1998, the consortia are working with suppliers in 1997 to demonstrate the performance of equipment and materials. Availability of test wafers and measurement tools is critical to the early development of process equipment. Wafers conforming to SEMI's development wafer standards are

available from many suppliers in quantities consistent with demand in 1997. The progress on wafer technology for device manufacturing quality is projected by suppliers to meet the start-up schedule, and is being evaluated by consortia. The majority of required metrology tools are now available to support blanket films and bulk materials characterization. The patterned wafer defect detection, critical dimension and overlay measurement capabilities have roadmaps which coincide with lithographic exposure tools, and are not available to support developing etch and chem-mechanical polish (CMP) equipment.

Fab equipment is generally being developed to meet the 1997 demonstration target. At least one supplier of each major tool type except lithography exposure will have a product of maturity suitable for process performance testing. While most suppliers have begun aggressive programs for 300 mm, equipment from some suppliers will not be ready for manufacturing performance testing until 1998. While these suppliers have made a business decision to delay development based upon perceived customer purchase timing, data available from earlier demonstrations will drive greater improvement of the equipment with more competitive schedules. The level of tool maturity that results from each of these strategies will be apparent at the time of purchasing decisions.

The exposure equipment schedules are targeting 1998 start-up of device operations, leaving suppliers of other patterned process and measurement equipment with less than optimum capability to characterize their products during development. Competitive pressure among suppliers from increasing availability of 300 mm equipment in 1997, as well as the announcement of early 300 mm facilities in 1998, will drive demand for critical path lithography tools. If suppliers of this equipment expect to provide reliable products which integrate with the balance of the fab tool set, the development of their large wafer capability will begin this year.

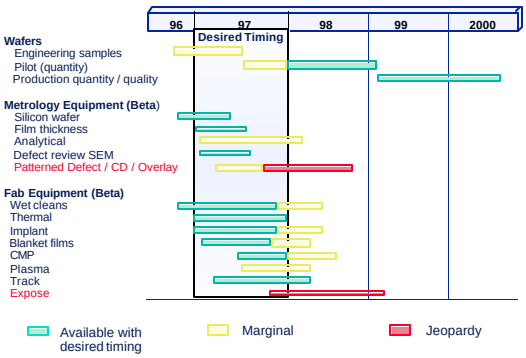

Figure 13. I300I Survey of Global Supplier Product Development Roadmaps

Conclusion

Increasing wafer sizes periodically has been a key component of the semiconductor industry's long record of productivity growth. Projected demand for silicon area and historic trends in wafer size conversion have been analyzed and compared to the current transition for 300 mm. This wafer size transition is driven, like those before it, by the need to reduce manufacturing cost on increassingly large devices. Given the accelerating state of mobilization for 300 mm among equipment and materials suppliers, the entire industry is on track to do what it has always done: continue the productivity growth that fuels the expansion of demand for its products.

References

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